# DATA SHEET

# SAA1057
## Radio tuning PLL frequency synthesizer

Product specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

## GENERAL DESCRIPTION

The SAA1057 is a single chip frequency synthesizer IC in $I^2L$ technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

### Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage ranges | $V_{CC1}$ | 3,6 to 12 | | V |
| | $V_{CC2}$ | 3,6 to 12 | | V |
| | $V_{CC3}$ | $V_{CC2}$ to 31 | | V |
| Supply currents | $I_{CC1} + I_{CC2}$ | typ. | 18 | mA |
| | $I_{CC3}$ | typ. | 0,8 | mA |
| Input frequency ranges | | | | |
| at pin FAM | $f_{FAM}$ | 512 kHz to 32 | | MHz |
| at pin FFM | $f_{FFM}$ | 70 to 120 | | MHz |
| Maximum crystal input frequency | $f_{XTAL}$ | > | 4 | MHz |
| Operating ambient temperature range | $T_{amb}$ | –25 to + 80 | | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT102H); SOT102-1; 1996 September 2.

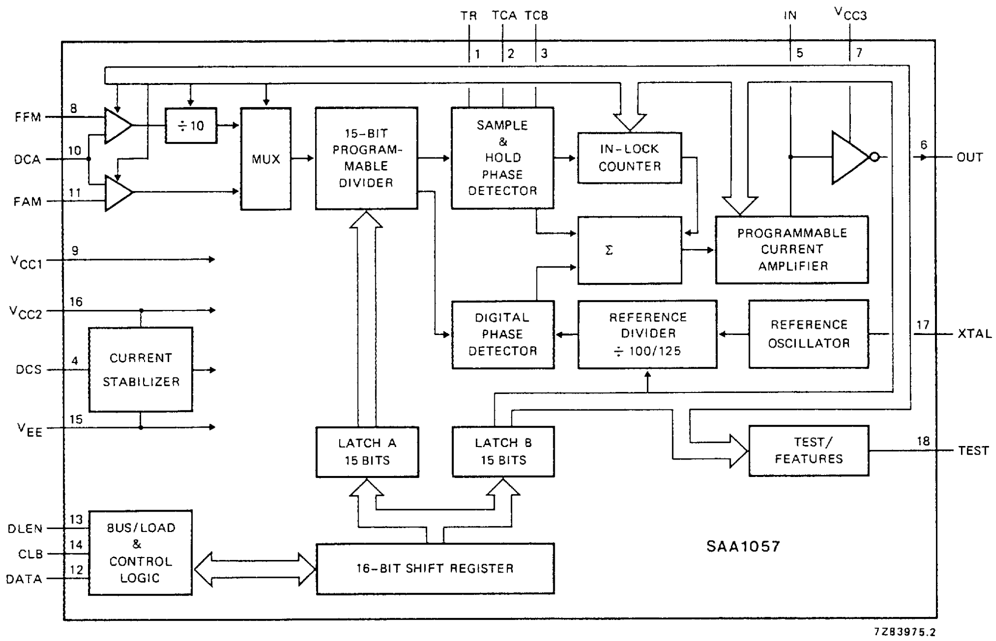



Fig.1 Block diagram.

## GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig.3). Latch B contains the control information.

## OPERATION DESCRIPTION

### Control information

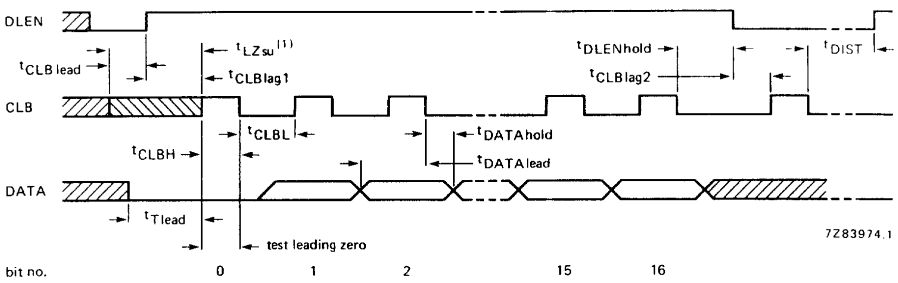
The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig.3.

| | |
|---|---|
| FM | FM/AM selection; ‘1’ = FM, ‘0’ = AM |
| REFH | reference frequency selection; ‘1’ = 1,25 kHz, ‘0’ = 1 kHz (sample and hold phase detector) |
| CP3 | control bits for the programmable current amplifier (see section Characteristics) |
| CP2 | |
| CP1 | |
| CP0 | |
| SB2 | enables last 8 bits (SLA to T0) of data word B; ‘1’ = enables, ‘0’ = disables; when programmed ‘0’, the last 8 bits of data word B will be set to ‘0’ automatically |
| SLA | load mode of latch A; ‘1’ = synchronous, ‘0’ = asynchronous |
| PDM1 | phase detector mode |
| PDM0 | |

| PDM1 | PDM0 | digital phase detector |
|---|---|---|
| 0 | X | automatic on/off |
| 1 | 0 | on |
| 1 | 1 | off |

| | |
|---|---|
| BRM | bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); ‘1’ = current switched; ‘0’ = current always on |
| T3 | test bit; must be programmed always ‘0’ |
| T2 | test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin |
| T1 | test bit; must be programmed always ‘0’ |
| T0 | test bit; selects the output of the programmable counter to the TEST pin |

| T3 | T2 | T1 | T0 | TEST (pin 18) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | reference frequency |
| 0 | 0 | 0 | 1 | output programmable counter |
| 0 | 1 | 0 | 1 | output in-lock counter<br>‘0’ = out-lock<br>‘1’ = in-lock |




(1) During the zero set-up time ($t_{LZsu}$) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines.

Fig.2 BUS format.

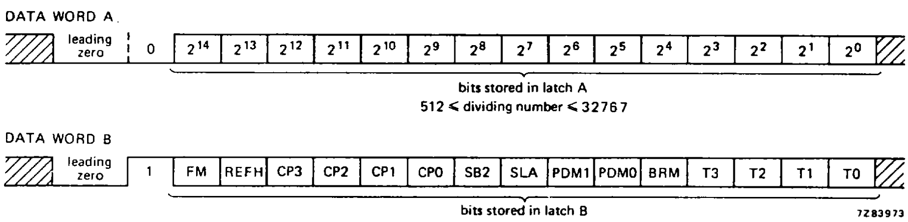



Fig.3 Bit organization of data words A and B.

## PINNING

| | | |
|---|---|---|
| 1 | TR | resistor/capacitors for sample and hold circuit |
| 2 | TCA | |
| 3 | TCB | |
| 4 | DCS | decoupling of supply |
| 5 | IN | input of output amplifier |
| 6 | OUT | output of output amplifier |
| 7 | $V_{CC3}$ | positive supply voltage of |
| | | output amplifier |
| 8 | FFM | FM signal input |
| 9 | $V_{CC1}$ | positive supply voltage of |
| | | high frequency logic part |
| 10 | DCA | decoupling of input |
| | | amplifiers |
| 11 | FAM | AM signal input |
| 12 | DATA | BUS |
| 13 | DLEN | |
| 14 | CLB | |
| 15 | $V_{EE}$ | ground |
| 16 | $V_{CC2}$ | positive supply voltage of low frequency logic part and analogue part |
| 17 | XTAL | reference oscillator input |
| 18 | TEST | test output |

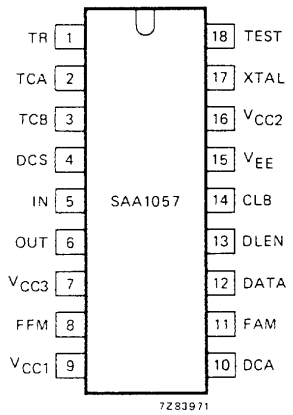



Fig.4 Pinning diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage; logic and analogue part | $V_{CC1}$; $V_{CC2}$ | –0,3 to 13,2 | V |
| Supply voltage; output amplifier | $V_{CC3}$ | $V_{CC2}$ to +32 | V |
| Total power dissipation | $P_{tot}$ | max. 800 | mW |
| Operating ambient temperature range | $T_{amb}$ | –30 to +85 | °C |
| Storage temperature range | $T_{stg}$ | –65 to +150 | °C |

## CHARACTERISTICS

$V_{EE}$ = 0 V; $V_{CC1}$ = $V_{CC2}$ = 5 V; $V_{CC3}$ = 30 V; $T_{amb}$ = 25 °C; unless otherwise specified

| | SYMBOL | MIN. | TYP. | MAX. | | CONDITIONS |
|---|---|---|---|---|---|---|
| Supply voltages | $V_{CC1}$ | 3,6 | 5 | 12 | V | |
| | $V_{CC2}$ | 3,6 | 5 | 12 | V | |
| | $V_{CC3}$ | $V_{CC2}$ | – | 31 | V | |
| Supply currents(6) | | | | | | |
| AM mode | $I_{tot}$ | – | 16 | – | mA | $I_{tot} = I_{CC1} + I_{CC2}$ in-lock: |
| FM mode | $I_{tot}$ | – | 20 | – | mA | BRM = ‘1’; PDM = ‘0’ |
| | $I_{CC3}$ | 0,3 | 0,8 | 1,2 | mA | $I_{OUT}$ = 0 |
| Operating ambient temperature | $T_{amb}$ | –25 | – | +80 | °C | |
| **RF inputs (FAM, FFM)** | | | | | | |
| AM input frequency | $f_{FAM}$ | 512 kHz | – | 32 | MHz | |
| FM input frequency | $f_{FFM}$ | 70 | – | 120 | MHz | |
| Input voltage at FAM | $V_{i\,(rms)}$ | 30 | – | 500 | mV | |
| Input voltage at FFM | $V_{i\,(rms)}$ | 10 | – | 500 | mV | |
| Input resistance at FAM | $R_i$ | – | 2 | – | kΩ | |
| Input resistance at FFM | $R_i$ | – | 135 | – | Ω | |
| Input capacitance at FAM | $C_i$ | – | 3,5 | – | pF | |
| Input capacitance at FFM | $C_i$ | – | 3 | – | pF | |
| Voltage ratio allowed between selected and non-selected input | $V_s/V_{ns}$ | – | –30 | – | dB | |
| **Crystal oscillator (XTAL)** | | | | | | see note 1 |
| Maximum input frequency | $f_{XTAL}$ | 4 | – | – | MHz | |
| Crystal series resistance | $R_s$ | – | – | 150 | Ω | |
| **BUS inputs (DLEN, CLB, DATA)** | | | | | | |
| Input voltage LOW | $V_{IL}$ | 0 | – | 0,8 | V | |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | $V_{CC1}$ | V | |
| Input current LOW | $-I_{IL}$ | – | – | 10 | µA | $V_{IL}$ = 0,8 V |
| Input current HIGH | $I_{IH}$ | – | – | 10 | µA | $V_{IH}$ = 2,4 V |
| **BUS inputs timing** (DLEN, CLB, DATA) | | | | | | see also Fig.2 and note 2 |
| Lead time for CLB to DLEN | $t_{CLBlead}$ | 1 | – | – | µs | |
| Lead time for DATA to the first CLB pulse | $t_{Tlead}$ | 0,5 | – | – | µs | |
| Set-up time for DLEN to CLB | $t_{CLBlag1}$ | 5 | – | – | µs | |
| CLB pulse width HIGH | $t_{CLBH}$ | 5 | – | – | µs | |
| CLB pulse width LOW | $t_{CLBL}$ | 5 | – | – | µs | |

| | SYMBOL | MIN. | TYP. | MAX. | | CONDITIONS |
|---|---|---|---|---|---|---|
| Set-up time for DATA to CLB | $t_{DATAlead}$ | 2 | – | – | µs | |
| Hold time for DATA to CLB | $t_{DATAhold}$ | 0 | – | – | µs | |
| Hold time for DLEN to CLB | $t_{DLENhold}$ | 2 | – | – | µs | |
| Set-up time for DLEN to CLB load pulse | $t_{CLBlag2}$ | 2 | – | – | µs | |
| Busy time from load pulse to next start of transmission | $t_{DIST}$ | 5 | – | – | µs | next transmission after word ‘B’ to other device |
| Busy time | | | | | | or |
| asynchronous mode | $t_{DIST}$ | 0,3 | – | – | ms | next transmission to SAA1057 after word ‘A’ (see also note 5) |
| synchronous mode | $t_{DIST}$ | 1,3 | – | – | ms | |
| **Sample and hold circuit** (TR, TCA, TCB) | | | | | | see also notes 3; 4 |
| Minimum output voltage | $V_{TCA}$, $V_{TCB}$ | – | 1,3 | – | V | |
| Maximum output voltage | $V_{TCA}$, $V_{TCB}$ | – | – | $V_{CC2}$–0,7 | V | |
| Capacitance at TCA | $C_{TCA}$ | – | – | 2,2 | nF | REFH = ‘1’ |
| (external) | $C_{TCA}$ | – | – | 2,7 | nF | REFH = ‘0’ |
| Discharge time at TCA | $t_{dis}$ | – | – | 5 | µs | REFH = ‘1’ |
| | $t_{dis}$ | – | – | 6,25 | µs | REFH = ‘0’ |
| Resistance at TR | $R_{TR}$ | 100 | – | – | Ω | external |
| Voltage at TR during discharge | $V_{TR}$ | – | 0,7 | – | V | |
| Capacitance at TCB | $C_{TCB}$ | – | – | 10 | nF | external |
| Bias current into TCA, TCB | $I_{bias}$ | – | – | 10 | nA | in-lock |
| **Programmable current amplifier (PCA)** | | | | | | |
| Output current of the dig. phase detector | $\pm I_{dig}$ | – | 0,4 | – | mA | |
| Current gain of PCA | | | | | | |
| CP3 CP2 CP1 CP0 | | | | | | |
| P1 0 0 0 0 | $G_{P1}$ | – | 0,023 | – | | $V_{CC2} \geq 5$ V (only for P1) |
| P2 0 0 0 1 | $G_{P2}$ | – | 0,07 | – | | |
| P3 0 0 1 0 | $G_{P3}$ | – | 0,23 | – | | |
| P4 0 1 1 0 | $G_{P4}$ | – | 0,7 | – | | |
| P5 1 1 1 0 | $G_{P5}$ | – | 2,3 | – | | |

| | SYMBOL | MIN. | TYP. | MAX. | | CONDITIONS |
|---|---|---|---|---|---|---|
| Ratio between the output current of S/H into PCA and the voltage on $C_{TCB}$ | $S_{TCB}$ | – | 1,0 | – | μA/V | |
| Offset voltage on TCB | $\Delta V_{TCB}$ | – | – | 1 | V | in-lock |
| **Output amplifier (IN, OUT)** | | | | | | |
| Input voltage | $V_{IN}$ | – | 1,3 | – | V | in-lock; equal to internal reference voltage |
| Output voltages | | | | | | |
| minimum | $V_{OUT}$ | – | – | 0,5 | V | $-I_{OUT}$ = 1 mA |
| maximum | $V_{OUT}$ | $V_{CC3}$–2 | – | – | V | $I_{OUT}$ = 1 mA |
| maximum | $V_{OUT}$ | $V_{CC3}$–1 | – | – | V | $I_{OUT}$ = 0,1 mA |
| Maximum output current | $\pm I_{OUT}$ | 5 | – | – | mA | $V_{OUT} = \frac{1}{2} V_{CC3}$ |
| **Test output (TEST)**(7) | | | | | | |
| Output voltage LOW | $V_{TL}$ | – | – | 0,5 | V | |
| Output voltage HIGH | $V_{TH}$ | – | – | 12 | V | |
| Output current OFF | $I_{Toff}$ | – | – | 10 | μA | $V_{TH}$ |
| Output current ON | $I_{Ton}$ | 150 | – | – | μA | $V_{TL}$ |
| **Ripple rejection**(8) | | | | | | |
| at $f_{ripple}$ = 100 Hz | | | | | | |
| $\Delta V_{CC1}/\Delta V_{OUT}$ | | – | 77 | – | dB | |
| $\Delta V_{CC2}/\Delta V_{OUT}$ | | – | 70 | – | dB | |
| $\Delta V_{CC3}/\Delta V_{OUT}$ | | – | 60 | – | dB | $V_{OUT} \leq V_{CC3}$–3 V |

**Notes**

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig.5. The values given in Fig.5 are a typical application example.
2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ $V_{CC2}$+0,3 when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ $V_{CC2}$+0,3 V.
4. Crystal oscillator frequency $f_{XTAL}$ = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (>17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 µs will be sufficient.
6. When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.
7. Open collector output.
8. Measured in Fig.6.

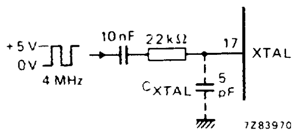



Fig.5 Circuit configuration showing external 4 MHz clock.

## APPLICATION INFORMATION

### Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

### Synchronous/asynchronous operation

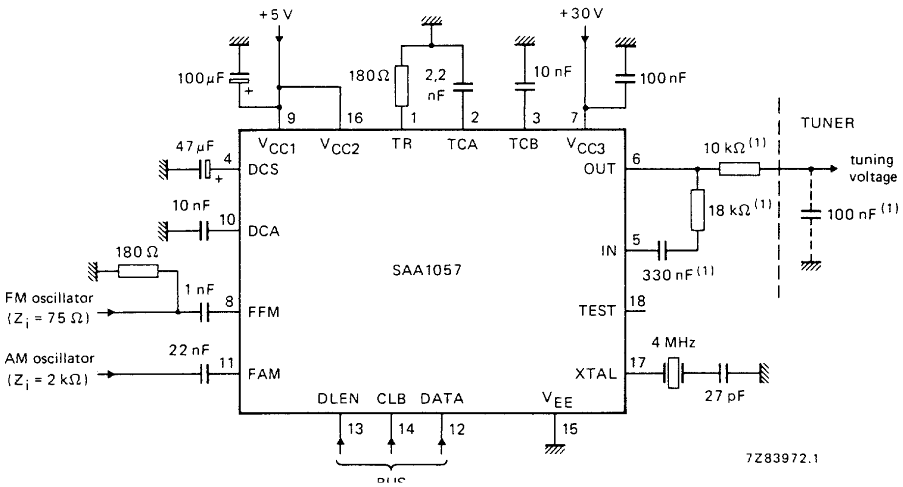
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

### Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage $V_{CC2}$ is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

### Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.

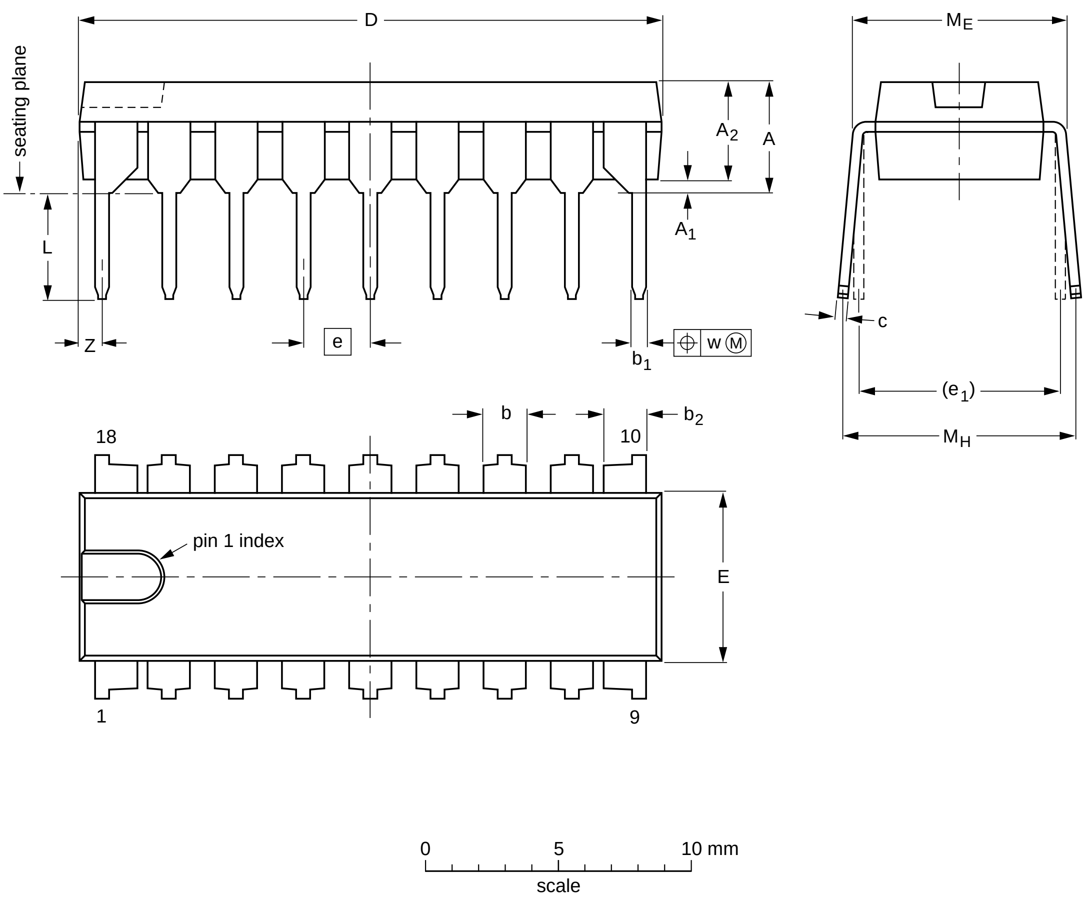



(1) Values depend on the tuner diode characteristics.

Fig.6 Application example of the SAA1057PLL frequency synthesizer module.

## PACKAGE OUTLINE

**DIP18: plastic dual in-line package; 18 leads (300 mil)** **SOT102-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 3.7 | 1.40<br>1.14 | 0.53<br>0.38 | 1.40<br>1.14 | 0.32<br>0.23 | 21.8<br>21.4 | 6.48<br>6.20 | 2.54 | 7.62 | 3.9<br>3.4 | 8.25<br>7.80 | 9.5<br>8.3 | 0.254 | 0.85 |
| inches | 0.19 | 0.020 | 0.15 | 0.055<br>0.044 | 0.021<br>0.015 | 0.055<br>0.044 | 0.013<br>0.009 | 0.86<br>0.84 | 0.26<br>0.24 | 0.10 | 0.30 | 0.15<br>0.13 | 0.32<br>0.31 | 0.37<br>0.33 | 0.01 | 0.033 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT102-1 | | | | | | ~~93-10-14~~<br>95-01-23 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.